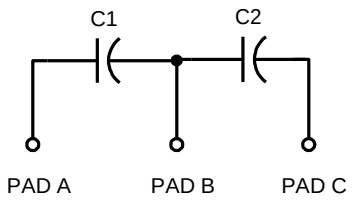
Dual 68pF Precision Thin-Film Capacitors

Features

- Ultra-low profile (0.18 mm height)
- Topside wirebonding pads
- Optional backside contact
- High quality LPCVD nitride dielectric
- Superior breakdown voltage performance
- Low ESR
- High Q
- Tolerances down to ±2%
- 100% electrically tested
- Topside passivation for pick and place handling
- Available as inked wafers or on wafer film frame
- RoHS compliant and Pb-free

Applications

- 13.56 MHz contactless smart cards
- RFID resonance circuits
- Chip-on-Board (COB) designs
- Known Good Die (KGD) programs



Description

The SiliconApps dual capacitor chip is designed for RFID applications requiring both a tuning and a detuning capacitance in a single chip. By connecting the internal capacitors either in series or singly the resonant frequency of the LC antenna circuit may easily be varied. The capacitance network is well suited for 13.56MHz ISO 15693 smart card applications, ISO 18000-3 RFID item management tags, and other applications that require precision, high frequency operation, and an ultra-thin profile.

The chip features topside wire bonding pads to support Chip-on-Board (COB) and Direct Chip Attachment (DCA) manufacturing flows. The middle electrical terminal (B) can also be contacted through the substrate if an optional backside gold (Au) metalization flow is selected. Capacitor layout is optimized to reduce effective series resistance (ESR) and to boost quality factor (Q). The entire chip is passivated with a silicon nitride topside layer to protect the die during pick and place handling.

SiliconApps capacitors use LPCVD silicon nitride as the capacitor dielectric. LPCVD outperforms the plasma-enhanced (PECVD) dielectrics used by other thin-film manufacturers, yielding a film of superior uniformity and electrical breakdown characteristics. The result is a rugged capacitor better suited to the transient voltage conditions of RFID antenna coil applications.

Custom capacitor layout, values, and tolerances are available as special orders. Please contact the factory at sales@SiliconApps.com

Part Numbering

SADC	D1	L	681	J	5W
Series	Layout	Dielectric	Capacitance Code	Capacitance Tolerance	Packaging Code
SADC	D1 = bond pad layout	L= LPCVD silicon nitride dielectric	Capacitance expressed in pF using 3 digit format. Third digit indicates powers of 10. Example: 68pF = '681'	G = ±2% J = ±5% K = ±10%	5W = 125 mm wafer 5WG = 125 mm wafer with backside gold 5F = 125 mm scribed wafer on film frame 5FG = 125 mm scribed wafer on film frame with backside gold

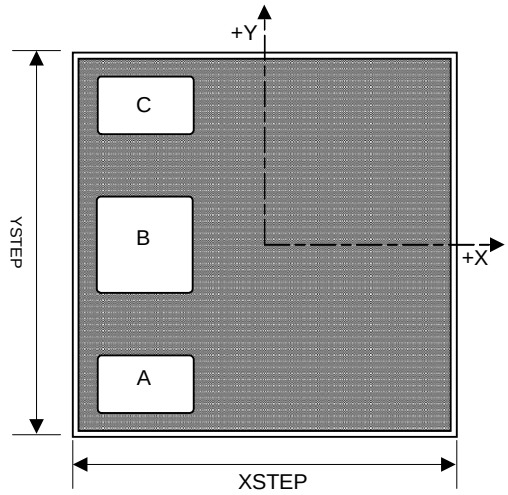
Electrical Specifications[1]

Parameter	Symbol	Conditions
Capacitance	C1, C2	1 MHz, 1 V rms, 100% electrically tested
Temperature Coefficient of Capacitance	TCC	+45 ±25 ppm/°C
Operating Temperature Range	TO	-55°C to +125°C
Insulation Resistance	IR	$> 10^{10}$
Aging	AR	No aging effect
Working Voltage	WV	Maximum continuous operating voltage
Breakdown Voltage	VB	> 1.5 X working voltage

Notes:

1) All measurements at 25°C unless otherwise specified.

Type D1 Capacitor Layout



Capacitance Ranges

Capacitance (pF)			Capacitance Code	Available Tolerances[2]	WV (volts)
C1	C2	C_{SERIES}			
68	68	34	680	G, J, K	30

Notes:
2) G = ±2%, J = ±5%, K = ±10%

Physical Dimensions

Parameter	Symbol	Dimension	Units
Capacitor Length (typical)[3]	L	0.95 / (0.0374)	mm / (inches)
Capacitor Width (typical)[3]	W	0.95 / (0.0374)	mm / (inches)
Capacitor Thickness	T	0.18 ±0.02 / (0.0071)	mm / (inches)
Die Stepping Distance on Wafer in X Direction	XSTEP	1000.0	microns
Die Stepping Distance on Wafer in Y Direction	YSTEP	1000.0	microns

Notes:
3) Final L, W dimensions depend on conditions and equipment used for wafer sawing. Values shown above reflect a 50 micron kerf.

Bond Pad Coordinates

Pad	Connection	Parameter	X	Y	Units
Pad A	C1 Electrode	Center of Bond Pad[4]	-310.0	-363.0	microns
		Width of Passivation Opening	250.0	150.0	microns
Pad B	C1 / C2 Shared Electrode + Substrate Connection	Center of Bond Pad[4]	-312.0	0.0	microns
		Width of Passivation Opening	250.0	250.0	microns
Pad C	C2 Electrode	Center of Bond Pad[4]	-310.0	363.0	microns
		Width of Passivation Opening	250.0	150.0	microns

Notes:
4) Pad locations are referenced to the center of the die. The +Y direction is away from the wafer flat.

Reference Applications

Manufacturer	Part Number	Description
Microchip	MCRF355	13.56MHzPassiveRFIDDevicewithAnti-CollisionFeature
Microchip	MCRF450	13.56MHzAnti-collisionRead/WritemicroID®devicewithnointernalresonantcapacitor
Microchip	MCRF450/7M	13.56MHZRFIDRead/WriteTaggingICinIOA2Module