PolySilicon Series Precision Thin-Film Capacitors – Format "A"

Features:

- Ultra-low profile (0.18 mm height)
- Dual topside wire-bonding pads
- Superior breakdown voltage performance
- High quality LPCVD nitride dielectric
- Capacitances from 20pF to 750pF
- Topside passivation for pick-and-place handling
- RoHS compliant and Pb-free

Applications:

- 125 kHz proximity access cards
- 135 kHz RFID transponders
- Multi-chip-module (MCM)
- Chip-on-Board (COB) designs
- System-in-Package (SIP) designs
- Known Good Die (KGD) programs
- Chip and wire applications

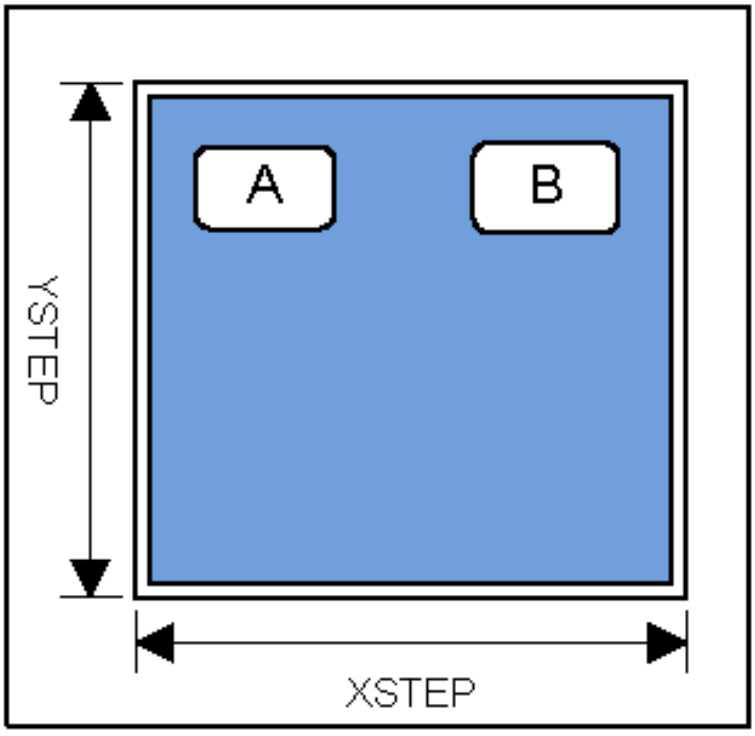
Product Description

The **SiliconApps** SAPC capacitors use state-of-the-art semiconductor wafer manufacturing process to achieve an extremely stable and low-profile thin-film capacitor based on a silicon nitride (Si3N4) dielectric. The capacitors are optimized for cost-sensitive applications where low profile and precision capacitance are required, such as 125 kHz security access card applications and RFID resonance circuits.

Each capacitor has two topside wire-bonding sites to support Chip-on-Board (COB) and Direct Chip Attachment (DCA) manufacturing flows. The capacitor comprises of a silicon nitride dielectric between a polysilicon lower electrode and an aluminum top electrode. This combination results in outstanding reliability and excellent stability over temperature.

An electrically isolated silicon substrate provides mechanical strength while allowing the use of either conductive or non-conductive die attach. The capacitors are passivated with an additional silicon nitride topside layer to protect the die during Pick and place handling. Custom capacitor layout, values and tolerances are available as special orders.

The available Capacitance (C) range for this format is 20pF to 750pF. The Breakdown Voltage (BV) varies depending on the capacitance value. The lower the C, higher the BV.



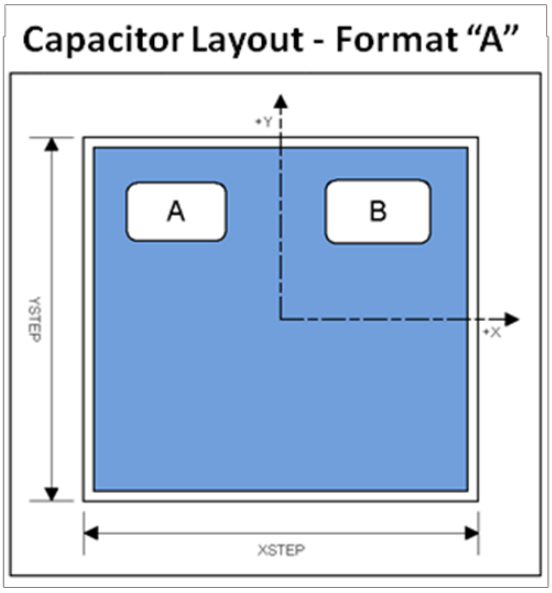
Electrical Specifications(1)

Parameter	Symbol	Conditions
Capacitance	C	1 MHz, 1 V rms, 100% electrically tested
Temperature Coefficient of Capacitance	TCC	+45 ±25 ppm/°C
Operating Temperature Range	T_{OP}	-55°C to +125°C
Insulation Resistance	IR	> 1010 ohms
Aging	AR	No aging effect
Working Voltage	WV	Maximum continuous operating voltage
Breakdown Voltage	V_{BR}	> 1.5 X Working Voltage

(1) All measurements at 25°C unless otherwise specified

ORDERING PART NUMBER					
SAPC	**330**	**K**	**7**	**A**	**W**
Product Family	**3-digit Capacitance Code**	**Capacitor Tolerance**	**Device Thickness**	**Back Metal for Die Attach (Typical thickness)**	**Package Type**
	Capacitance Code Examples: 068 = 68pF and 510 = 510pF	J = ±5%	9 = 9 mils	No Letter = Bare Silicon (No Back Metal)	W = Unsawn full 5" wafer
		K = ±10%	7 = 7 mils	A= Ti/Ni/Au (550A/4,000A/2,500A)	B = Diced and shipped on mylar/tape in Saw rings
		M = ±20%	6 = 6 mils	S = Ti/Ag (550A/5,000A)	P = Diced and shipped in Gelpak

Part Number Example: **SiliconApps** SAPC330K7AW is a PolySilicon Capacitor; 330pF ±10%; having 7-mils thick with Ti/Ni/Au back-metal and shipped as unsawn wafer



A & B are wire-bond pads

Physical Dimensions			
Parameter	**Symbol**	**Dimension**	**Units**
Capacitor Length (typical) (2)	L	0.94 / (0.0370)	mm / (inches)
Capacitor Width (typical) (2)	W	0.88 / (0.0346)	mm / (inches)
Capacitor Thickness	T	0.18 ±0.02 / (0.0071)	mm / (inches)
Die Stepping Distance on Wafer in X Direction	XSTEP	990	microns
Die Stepping Distance on Wafer in Y Direction	YSTEP	930	microns

(2) Final L, W dimensions depend on conditions and equipment used for wafer sawing. Values shown above reflect a 50 micron wide kerf.

Bond Pad Coordinates				
Pad	**Parameter**	**X**	**Y**	**Units**
Pad A	Center of Bond Pad (3)	-260	275	microns
	Width of Passivation Opening	250	150	microns
Pad B	Center of Bond Pad (3)	240	275	microns
	Width of Passivation Opening	260	160	microns

(3) Pad locations referenced to the center of the die. The +Y direction is away from the wafer flat